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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,722	06/24/2003	Keng L. Wong	P15985-110348-131862	3340

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SCHWABE, WILLIAMSON & WYATT, P.C.
PACWEST CENTER, SUITES 1600-1900
1211 SW FIFTH AVENUE
PORTLAND, OR 97204

EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,722	WONG ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are presented in the instant application according to the Applicants' filing on 06/24/2003.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Drawings Objection

2. The drawings are objected to because of lacking "Prior Art" label in figure 1.

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections/Minor Informalities

4. Claim 19 is objected to because of the following informalities:

Lines 4-5, there is no express antecedent basis for "the second input signal". It is suggested that "the" be changed to -- a -- .

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-14 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by sung et al. (U.S. Patent No. 6,218,876).

With respect to claim 1, Sung et al. discloses, in Fig. 2, a circuit comprising a) a first phase-locked loop (PLL) [52] to receive a first reference signal [100] and a first feedback signal [output from 120 to 110], and to produce a data clock signal [output from 120] having a first frequency based at least in part upon differences between the first reference signal and a first feedback signal, and b) a second PLL [54] coupled to the first PLL to receive a second reference signal and a second feedback signal, and to produce a second clock signal [output from 220] having a second frequency based at least in part upon differences between the second reference signal and the second feedback signal, the first feedback signal and the second reference signal being derived from the data clock signal and the second feedback signal being derived from the second clock signal.

With respect to claim 2, Sung et al. discloses, in Fig. 2, a first divide-by-N circuit [130] coupled to the first PLL circuit to divide the first frequency of the data clock signal by a first integer value N to produce the first feedback signal having a third frequency.

With respect to claim 3, Sung et al. discloses, in Fig. 2, a divide-by-M circuit [140] coupled between the first PLL circuit and the second PLL circuit to divide the first frequency of the data clock signal by an integer value M to produce the second reference signal.

With respect to claim 4, Sung et al. discloses, in Fig. 2, and column 4, lines 46-49, that the divide-by-M circuit is equipped to divide the first frequency of the data clock signal by a selected one of a factor of 4, 2 and 1.

With respect to claim 5, Sung et al. discloses, in Fig. 2, and column 4, lines 46-49, that the first divide-by-N circuit comprises a divide-by-4 circuit to divide the first frequency of the data clock signal by a factor of 4.

With respect to claim 6, Sung et al. discloses, in Fig. 2, and column 4, lines 46-49, a second divide-by-N circuit [230] coupled to the second PLL to divide the second frequency of the second clock signal by a second integer value N to produce the second feedback signal, wherein the second integer value N is selected from a group of integer values including a low integer value, and a high integer value that is less than two times the low integer value.

With respect to claim 8, Sung et al. discloses, in Fig. 2, a first signal path corresponding to the second reference signal, and a second signal path corresponding to the second feedback signal, wherein the first and second signal paths are equivalent in length.

With respect to claim 9, Sung et al. discloses, in Figs. 2 and 5, a microprocessor comprising a) a processor core [Fig. 5, item 304]; b) I/0 circuitry [Fig. 5, item 308]; and c) a clock generation circuit comprising a first phase-locked loop (PLL) circuit [Fig. 2, item 52] to produce a first output signal having a first frequency based at least in part upon a first reference signal and a first feedback signal derived from the first output signal, the first output signal to

be used as a data clock signal for the I/0 circuitry *(It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Therefore, this limitation has not been given patentable weight)*; and a second PLL circuit [Fig. 2, item 54] coupled to the first PLL to produce a second output signal having a second frequency based at least in pad upon a second reference signal derived from the first output signal and a second feedback signal derived from the second output signal, the second output signal to be used as a clock signal for the processor core *(It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Therefore, this limitation has not been given patentable weight)*.

With respect to claim 10, Sung et al. discloses, in Fig. 2, a first divide-by-N circuit [130] coupled to the first PLL circuit to divide the first frequency of the data clock signal by a first integer value N to produce the first feedback signal having a third frequency.

With respect to claim 11, Sung et al. discloses, in Fig. 2, a divide-by-M circuit [140] coupled between the first PLL circuit and the second PLL circuit to divide the first frequency of the data clock signal by an integer value M to produce the second reference signal.

With respect to claim 12, Sung et al. discloses, in Fig. 2, and column 4, lines 46-49, that the divide-by-M circuit is equipped to divide the first frequency of the data clock signal by a selected one of a factor of 4, 2 and 1.

With respect to claim 13, Sung et al. discloses, in Fig. 2, and column 4, lines 46-49, that

the first divide-by-N circuit comprises a divide-by-4 circuit to divide the first frequency of the data clock signal by a factor of 4.

With respect to claim 14, Sung et al. discloses, in Fig. 2, and column 4, lines 46-49, a second divide-by-N circuit [230] coupled to the second PLL to divide the second frequency of the second clock signal by a second integer value N to produce the second feedback signal, wherein the second integer value N is selected from a group of integer values including a low integer value, and a high integer value that is less than two times the low integer value.

With respect to claim 16, Sun et al. discloses, in Fig. 2, a first signal path corresponding to the second reference signal, and a second signal path corresponding to the second feedback signal, wherein the first and second signal paths are equivalent in length.

With respect to claim 17, Sung et al. discloses, in Fig. 2, a method comprising a) disposing a first [52] of at least two phase locked loops in a cascaded arrangement, such that the first PLL [52] produces a first output signal [output from 120] suitable for use as a data clock *(regarding the limitation* "suitable for use as a data clock"*; it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Therefore, this limitation has not been given patentable weight)* having a first frequency based at least in pad upon a first reference signal and a first feedback signal derived from the data clock signal, and b) disposing a second PLL [54] in communication with the first PLL, such that the second PLL produces a second output signal suitable for use as a core clock *(regarding the limitation* "suitable for use as a core clock"*; it has been held that a recitation with respect to the manner in which a claimed*

apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Therefore, this limitation has not been given patentable weight) having a second frequency based at least in pad upon a second reference signal derived from the first output signal and a second feedback signal derived from the second output signal.

With respect to claim 18, Sung et al. discloses, in Fig. 2, the first reference signal [100] being an external bus clock signal having a third frequency.

With respect to claim 19, Sung et al. discloses, in Fig. 2, the method including steps of a) dividing the data clock signal by a first integer value [130] to attain the first feedback signal, b) dividing the data clock signal by a second integer value [140] to attain the second input signal, and c) dividing the second output signal by a third integer value [230] to attain the second feedback signal.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung et al. (U.S. Patent No. 6,218,876).

With respect to claims 7 and 15, Sung et al. discloses all of the claimed limitations as expressly recited in claims 1 and 9, respectively, except for a bandwidth of the second PLL is at least three times greater than a bandwidth of the first PLL.

It would have been an obvious matter of preference or requirement bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed ratio of bandwidths between the second phase locked loop (PLL) and the first phase locked loop limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. Indeed, it has been held that optimization of the ratio of the bandwidth of the second PLL and the bandwidth of the first PLL limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d

1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results."

Citation of Relevant Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Ott (U.S. Patent No. 6,636,575) discloses a cascading PLL units for achieving rapid synchronization between digital communications systems.

Prior art Friedrich et al. (U.S. Patent No. 6,433,599) discloses a circuit for data signal recovery and clock signal regeneration.

Prior art Wilkinson (U.S. Patent No. 4,577,241) discloses an apparatus comprises a first PLL and a second PLL.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen
Examiner
Art Unit 2816

LMN